

Abstract of the Disclosure

[0055] Systems and methods for synchronizing multiple digital audio controller chips, wherein one of the chips is designated as a master and the other chips are designated as slaves. A common line connects all of the chips and is used to transmit synchronization signals from the master to the slaves. Each of the chips listens for an appropriate signal and, when the signal is detected, all of the chips simultaneously begin operation. In one embodiment, the synchronization signal comprises a transition on the shared line to an active state. The transition is repeated at fixed intervals and maintained in the active state for a fixed period in order to enable the chips to determine whether synchronization is being maintained. The signal may be sampled and/or filtered to improve reliability. The chips may be able to drive the shared line active to indicate that synchronization has been lost.